iSBC® MEM/312, 310, 320, 340
CACHE-BASED MULTIBUS® II RAM BOARDS

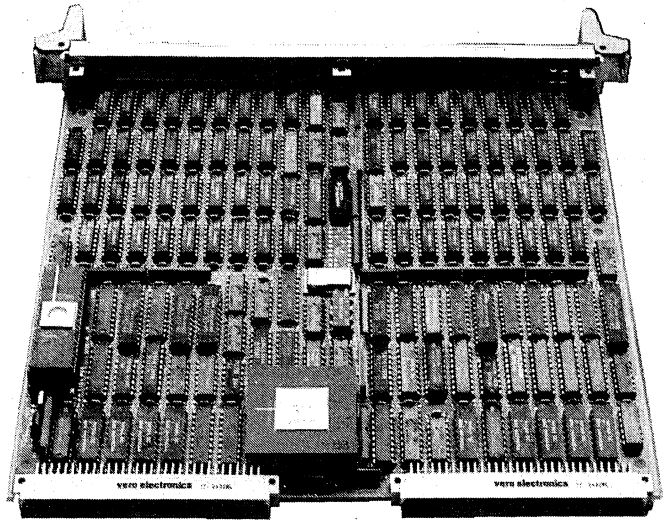
- **iSBC® MEM/3XX MULTIBUS® II Memory Boards Are High-Speed Cache-Based Boards with 8K Bytes of Cache RAM**
- **32-bit MULTIBUS® II Parallel System Bus (iPSB) and Local Bus Extension II (iLBX™ II Bus) Interface Support**
- **Zero Wait State Over iLBX™ on a Cache Hit, One Wait State for Cache Misses and Writes at 8 MHz**
- **Dual Port Memory with Four Versions Available:**

iSBC MEM/312	**½M Byte**
iSBC MEM/310	**1M Byte**
iSBC MEM/320	**2M Bytes**
iSBC MEM/340	**4M Bytes**

- **Double-high Eurocard Standard Form Factor, Pin and Socket DIN Connectors**
- **MULTIBUS II Software Interconnect Support for Dynamic Memory Configuration and Diagnostics with No Jumpers Necessary on the Board**
- **Built-In-Self-Test (BIST) Diagnostics On-Board with Both LED Indicators and Software Access to Error Information**
- **Automatic Memory Initialization at Power-Up and at Power-Fail Recovery**
- **Byte Parity Error Detection**

The iSBC MEM/312, 310, 320, 340 cache-based memory boards are the first Intel memory products to implement the MULTIBUS II system architecture. They have 32-bit architecture throughout, supporting 8-, 16-, and 32-bit central processors. The iSBC MEM/3XX (generally refers to this family of boards) memory boards are dual-ported, with access to the interfaces of both the MULTIBUS II Parallel System Bus (iPSB bus) and the iLBX II (Local Bus Extension).

In addition to the 32-bit memory transfer, the iSBC MEM/3XX high-speed cache control subsystem, standard on these boards, improves performance by allowing zero wait state read access over the iLBX II when data requested is in the cache memory.



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FUNCTIONAL DESCRIPTION

General

The iSBC MEM/312, 310, 320, 340 high-speed cache-based memory boards are physically and electrically compatible with the MULTIBUS II iPSB bus standard and the new iLBX II bus (Local Bus Extension) as outlined in the Intel MULTIBUS II specification. Figure 1 illustrates a typical multiprocessing MULTIBUS II system configuraton.

Architecture

The four main subsystems of the iSBC MEM/3XX boards are the cache controller subsystem, the cache memory subsystem, the DRAM memory subsystem, and the interconnect space subsystem (see Figure 2). The following sections describe these subsystems and their capabilities in more detail.

Cache Memory Capabilities

The cache memory system is designed around the 32-bit architecture of the main memory system and reduces read access timers. The 8K Bytes of 45 nsec SRAM allows zero wait state read accesses over the iLBX II bus when data requested is in the cache memory (cache hit). A cache hit takes only two iLBX II bus clocks (250 nsec at 8 MHz).

Each entry in the 8K Byte cache memory subsystem consists of a data field of 32-bits and a tag field of up to 9-bits (depending on board DRAM size). Each byte in the main memory DRAM array directly maps to one and only one entry on the cache array. This direct mapped cache array along with tag labels ensure data integrity and accurate identification of cache hits. The cache memory size and simple but effective replacement algorithm is designed to optimize both the probability of cache hits and the CPU bus utilization. On any miss or write access, the contents of one cache entry are updated to maintain consistency with the corresponding entry in the DRAM memory array.

Dual Port DRAM Capabilities

The iSBC MEM/312 module contains ½M Byte of read/write memory using 64K dynamic RAM compo-

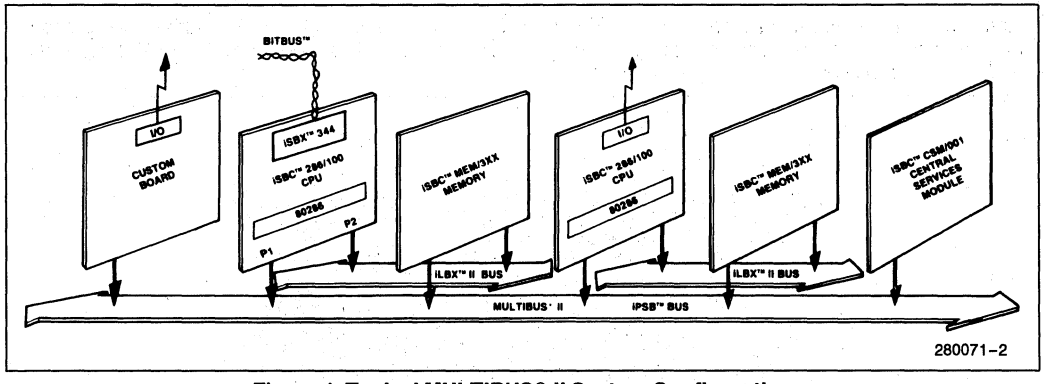

Figure 1. Typical MULTIBUS® II System Configuration

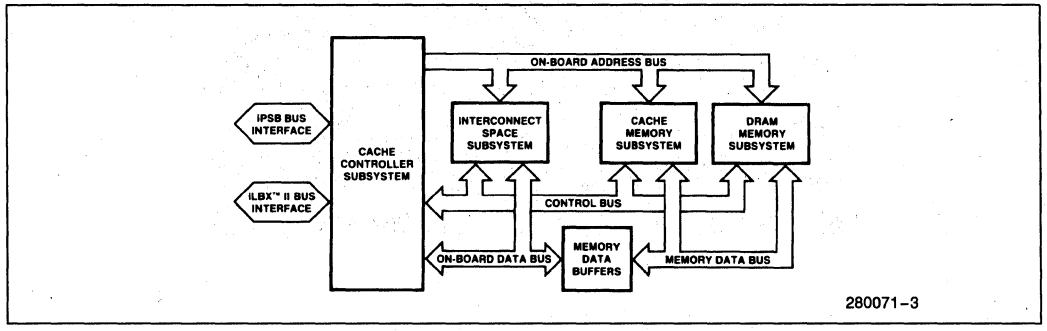

Figure 2. iSBC® MEM/3XX Board Block Diagram

nents. The iSBC MEM/310, MEM/320 and MEM/340 modules respectively contain 1M Byte, 2M Bytes and 4M Bytes of read/write memory using 256K dynamic RAM components.

The dual port capability of the iSBC MEM/3XX boards allows 32-bit access from either the iPSB bus interface or the iLBX II bus interface (see Figure 1). Due to the simple arbitration nature of the iLBX II bus interface and the cache memory subsystem, the iSBC MEM/3XX family allows optimal access to 20M Bytes of DRAM on the iLBX II bus.

System Memory Size

Using this series of memory boards the maximum system memory capacity based on one CPU board and 19 memory boards is 76M Bytes on the iPSB bus. The memory partitioning is independent for the iPSB bus interface and the iLBX II bus interface.

The start address can be on any 64K Byte boundary on the iPSB bus and any 64K Byte boundary on the iLBX II bus. Software configures the start and ending addresses through the interconnect space. No jumpers are needed.

Interconnect Space Capabilities

The iSBC MEM/3XX board module has a set of interconnect registers which allow the system software to dynamically configure and test the status of the memory board, replacing hardwired jumper functions. This interconnect subsystem also provides control and access to the Built-In-Self-Test (BIST) features. During power-up reset, the iSBC MEM/3XX board initializes the memory and cache, sets all interconnect registers to their default values and performs a self-test. Error information from both Built-In-Self-Test (BIST) and parity checking is indicated in front panel LEDs and recorded in interconnect space registers accessible to software.

Built-In-Self-Test (BIST)

Self-test/diagnostics have been built into the heart of the MULTIBUS II system. These confidence tests and diagnostics improve reliability and reduce manufacturing and maintenance costs. LED 1 (labelled BIST) is used to indicate the status of the Built-In Self Test. It is turned on when the BIST starts running and is turned off when the BIST completes successfully. The Built-In-Self-Test performed by the on-board microcontroller at power-up or at software command are:

1. **EPROM Checksum:**

   This test performs a checksum test on its internal EPROM to check operation of the 8751 microcontroller.

2. **Cache Data Test:**

   The microcontroller performs a sliding ones test on the cache memory in hit-only mode.

3. **Cache Address Test:**

   This test verifies that the cache address path is working properly.

4. **Refresh Check:**

   This test performs RAM test on a small portion of DRAM with an elapsed time between the write operation and the verification of the data.

5. **Dynamic RAM Address Test:**

   This test performs Address Rippled RAM test on the board memory (MISS ONLY operation mode).

6. **Dynamic RAM Data Test:**

   This test runs an AA-55 data pattern to check the DRAM data path.

7. **Parity Test:**

   This test injects parity errors in the DRAM array and then verifies that the board detects these errors.

These tests are described in detail in the User's Manual, Section 9-23.

Memory Initialization and Reset

Memory is initialized automatically during power-up. All bytes are set to 00.

Error Detection Using Byte Parity

Parity will detect all single bit parity errors on a byte parity basis and many muiltiple bit errors. LED 2 (labelled Parity) is used to indicate parity errors. LED 2 is turned on when a parity error is detected and turned off when the parity status register within interconnect space is cleared. This same LED turns on and off during power-up to verify operatoin of the LED.

Error information is recorded in interconnect space so it is accessible to software for error reporting.

SPECIFICATIONS

Word Size Supported

8-, 16-, 24-, and 32-bits

Memory Size

½ Megabyte (iSBC MEM/312) board
1 Megabyte (iSBC MEM/310) board
2 Megabytes (iSBC MEM/320) board
4 Megabytes (iSBC MEM/340) board

Access Times (All Densities)

MULTIBUS II Parallel System Bus—iPSB (@ 10 MHz)

Read: 562 ns (avg.)
775 ns (max.)

Write: 662 ns (avg.)
775 ns (max.)

NOTE:
Average access times assume 80% cache hit rates

iLBX™ II Bus—Local Bus Extension

Read: 250 ns (min.)
275 ns (avg.)
375 ns (max.)

Write: 375 ns (avg.)
375 ns (max.)

Base Address

iPSB Bus—any 64K Bytes boundary
iLBX II Bus—any 64K Bytes boundary

Power Requirements

Voltage: 5V DC ±5%

Product	Current
iSBC MEM/312 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/310 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/320 Board	3.5 A (typ) 6.0 A (max)
iSBC MEM/340 Board	4.1 A (typ) 6.7 A (max)

ENVIRONMENTAL REQUIREMENTS

Temperature: (inlet air) at 200 LFM airflow over boards
Non-Operating: −40 to +70°C
Operating: 0 to +55°C

Humidity: Non-operating: 95% RH @ 55°C
Operating: 90% RH @ 55°C

Physical Dimensions

The iSBC MEM/3XX boards meet all MULTIBUS II mechanical specifications as presented in the MULTIBUS II specification (#146077).

Double High Eurocard Form Factor:

Depth: 220 mm (8.6 in.)
Height: 233 mm (9.2 in.)
Front Panel Width: 20 mm (0.784 in.)

Weight:

iSBC MEM/312 board: 6720 gm (24 oz.)
iSBC MEM/310 board: 6160 gm (22 oz.)
iSBC MEM/320 board: 6720 gm (24 oz.)
iSBC MEM/340 board: 10080 gm (36 oz.)

Reference Manuals

iSBC MEM/3XX Board Manual (#146707-001)

Intel MULTIBUS II Bus Architecture Specification (#146077)

Manuals may be ordered from any Intel Sales Representative, Distributor Office, or from the Intel Literature Department. 3065 Bowers Ave., Santa Clara, CA 95051.

Ordering Information

Part Number	Description
iSBC MEM/312	½M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/310	1M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/320	2M Byte Cache Based MULTIBUS II RAM Board
iSBC MEM/340	4M Byte Cache Based MULTIBUS II RAM Board